Data Sheet

COMLINEAR® CLC2550, CLC4550

Low Power, Low Offset, 2V to 36V Comparators

FEATURES

- 2mV input offset voltage
- 25nA input bias current
- ±5nA input offset current
- 0.9mA supply current
- CMIR includes ground
- 200mV output saturation voltage at 4mA
- 2V to 36V single supply voltage range
- ±1V to ±18V dual supply voltage range
- Open collector output
- Differential input voltage range equals the power supply voltage
- CLC2550: improved replacement for industry standard LM393
- CLC4550: Improved replacement for industry standard LM339
- CLC2550: Pb-free SOIC-8
- CLC4550: Pb-free SOIC-14

APPLICATIONS

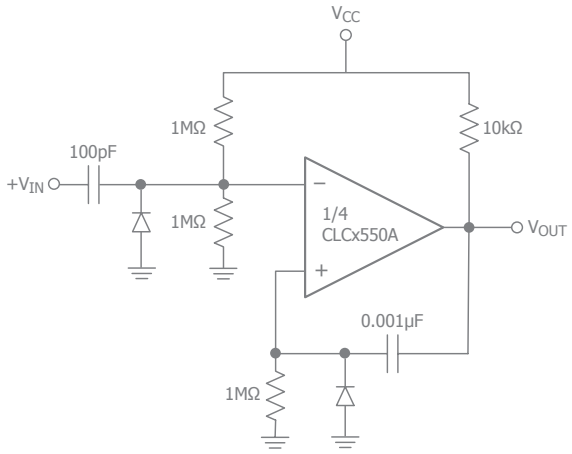
- Battery charger
- Cordless telephone
- Switching power supply
- DC-DC module
- PC motherboard
- Communication equipment
- Widerange VCO
- Squarewave and time delay generators
- MOS clock timers
- High voltage digital logic gates
- Multivibrators

General Description

The COMLINEAR CLC2550 (dual) and CLC4550 (quad) are precision voltage comparators with a typical offset of 2mV and high gain (200V/mV). These comparators also offer an input common-mode voltage range that includes ground.

The COMLINEAR CLC2550, and CLC4550 operate from a wide supply voltage range of ±1V to ±18V, or from a single supply range of 2V to 36V. These comparators are available in Pb-free, RoHS compliant SOIC-8 and SOIC-14 packages. They operate over the industrial temperature range of -40°C to +85°C.

Typical Application - One Shot Multivibrator



Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC2550ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
CLC4550ISO14X	SOIC-14	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

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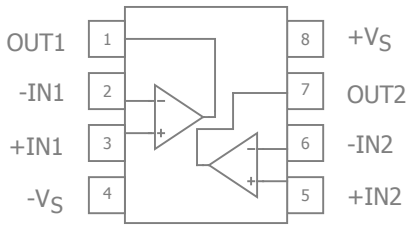
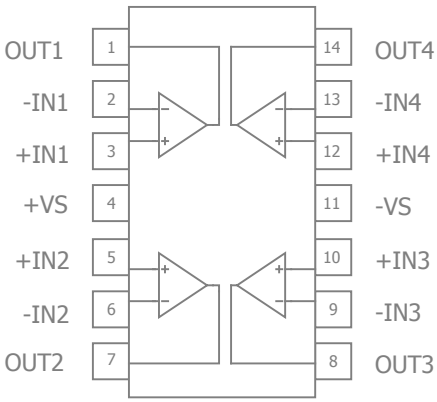
CLC2550 Pin Configuration



CLC4550 Pin Configuration



CLC2550 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

CLC4550 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	40	V
Differential Input Voltage		40	V
Input Voltage	-0.3	40	V
Input Current (V_{IN} < -0.3V) (1)		50	mA
Output Short Circuit Current to Ground	Continuous		
Power Dissipation (T_A = 25°C) - SOIC-8		660	mW
Power Dissipation (T_A = 25°C) - SOIC-14		890	mW

Notes:
1. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 V_{DC} (at 25°C).

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
SOIC-8		100		°C/W
SOIC-14		88		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2 (±1)		36 (±18)	V

Electrical Characteristics

T_A = 25°C (if **bold**, T_A = -40 to +85°C), V_S = +5V, $-V_S$ = GND unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Performance						
V_{IO}	Input Offset Voltage	V_{OUT} = 1.4V, R_S = 0Ω, V_S = 5V to 30V		2	5	mV
					7	mV
I_b	Input Bias Current	V_{CM} = 0V		25	250	nA
					400	nA
I_{OS}	Input Offset Current	V_{CM} = 0V		5	50	nA
					200	nA
CMIR	Common Mode Input Range (3)	$+V_S$ = 30V	0		$+V_S$ - 1.5	V
VG	Voltage Gain	$+V_S$ = 15V, R_L = ≥15kΩ, V_{OUT} = 1V to 11V	50	200		V/mV
I_S	Supply Current, CLC2550	R_L = ∞, $+V_S$ = 30V		0.7	1.7	mA
					3.0	mA
		R_L = ∞, $+V_S$ = 5V		0.6	1.0	mA
					2.0	mA
	Supply Current, CLC4550	R_L = ∞, $+V_S$ = 30V		1.2	2.5	mA
					3.0	mA
		R_L = ∞, $+V_S$ = 5V		0.9	2.0	mA
					3.0	mA
Time Domain Response						
t_{RLS}	Large Signal Response Time	V_{IN} = TTL logic swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ		200		ns
t_R	Response Time	V_{RL} = 5V, R_L = 5.1kΩ, 5mV overdrive		1.3		µs
		V_{RL} = 5V, R_L = 5.1kΩ, 10mV overdrive		0.9		µs
		V_{RL} = 5V, R_L = 5.1kΩ, 15mV overdrive		0.8		µs
Output Characteristics						
I_{SINK}	Output Sink Current	V_{IN+} = 0V, V_{IN-} = 1V, V_{OUT} = 1.5V	6.0	16		mA
I_{LEAK}	Output Leakage Current	V_{IN+} = 1V, V_{IN-} = 0V, V_{OUT} = 5V		0.1		nA
		V_{IN+} = 1V, V_{IN-} = 0V, V_{OUT} = 30V			**1**	µA
V_{SAT}	Saturation Voltage	V_{IN+} = 0V, V_{IN-} = 1V, I_{SINK} ≤ 4mA		200	400	mV
					500	mV

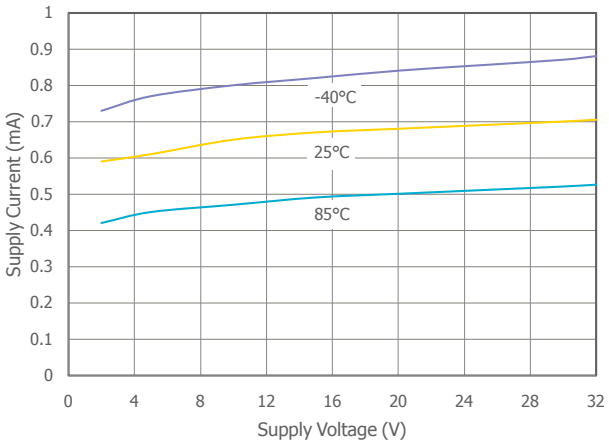
Notes:

1. 100% tested at 25°C
2. Limits over the full temperature range are guaranteed by design.
3. The input common mode voltage of either input signal voltage should be kept > 0.3V at 25°C. The upper end of the common-mode voltage range is $+V_S$ - 1.5V at 25°C, but either or both inputs can go to +18V without damages, independent of the magnitude of V_S.

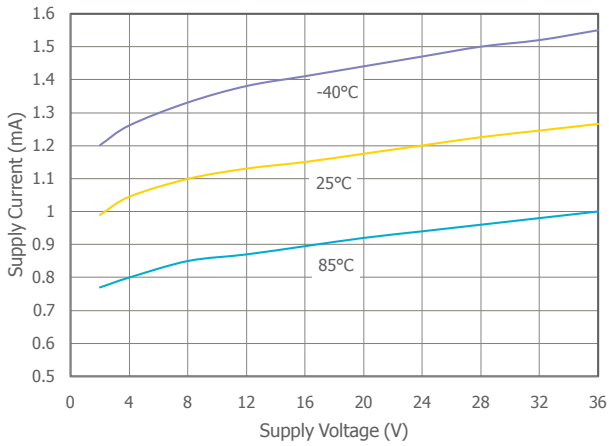
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, $-V_S$ = GND unless otherwise noted.

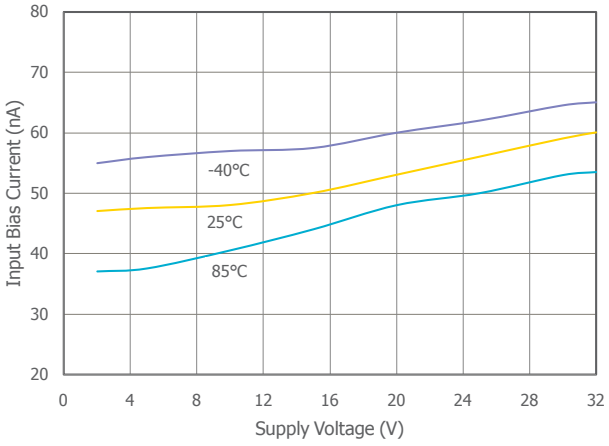
Supply Current vs. Supply Voltage (CLC2550)



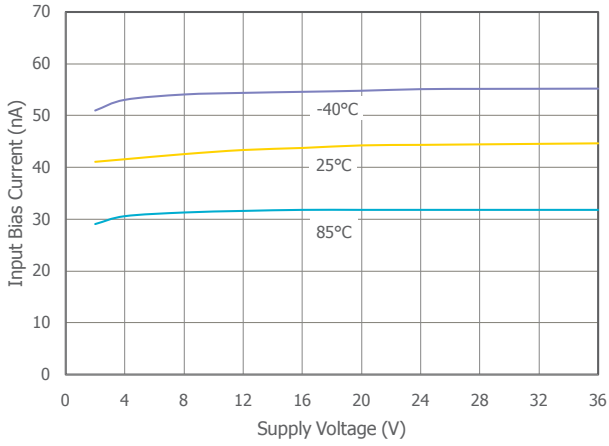
Supply Current vs. Supply Voltage (CLC4550)



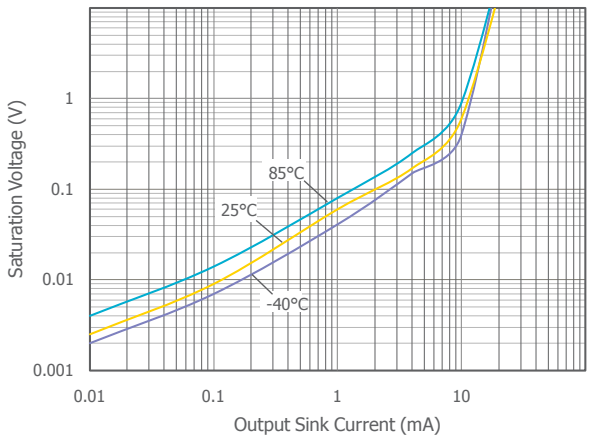
Supply Voltage vs. Input Bias Current (CLC2550)



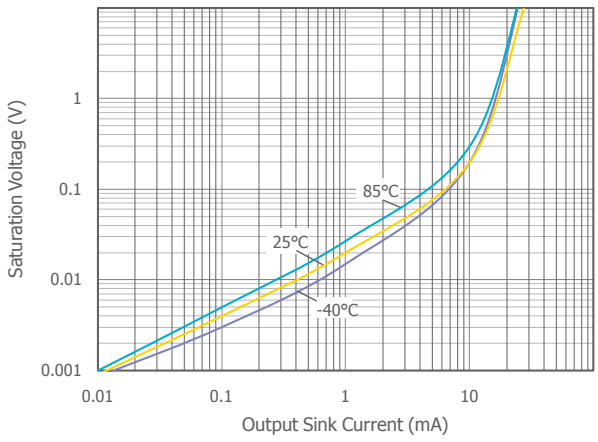
Supply Voltage vs. Input Bias Current (CLC4550)



Output Sink Current vs. Saturation Voltage (CLC2550)



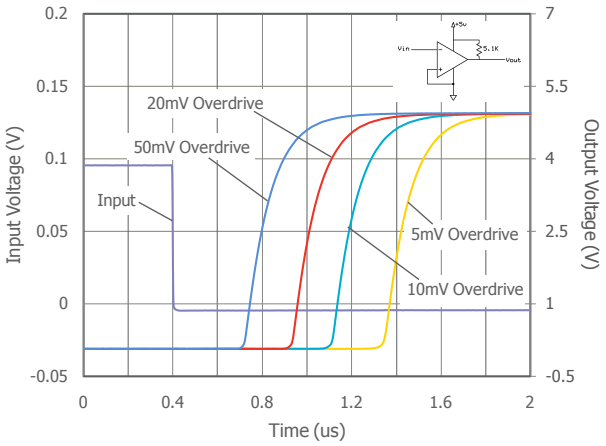
Output Sink Current vs. Saturation Voltage (CLC4550)



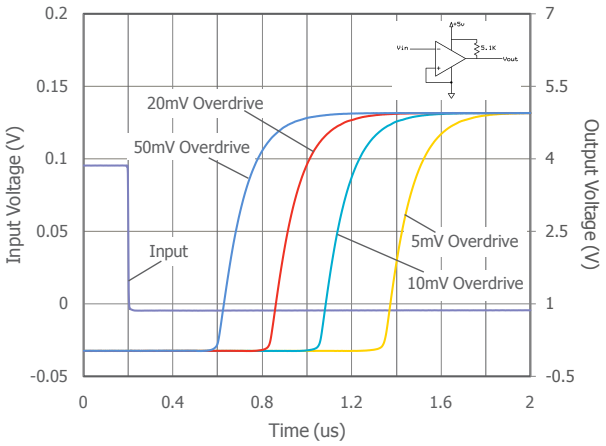
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, -V_S = GND unless otherwise noted.

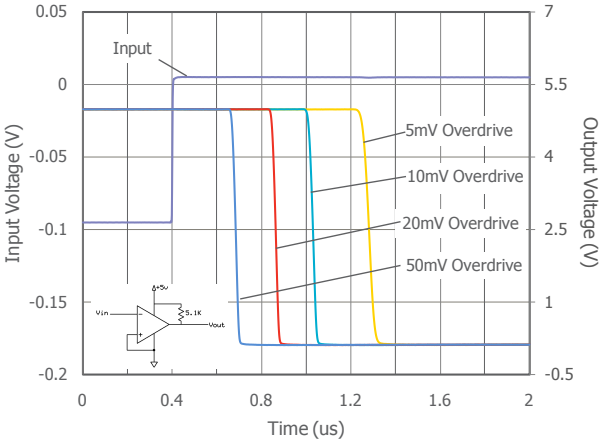
Response Time vs. Input Overdrive - Positive (CLC2550)



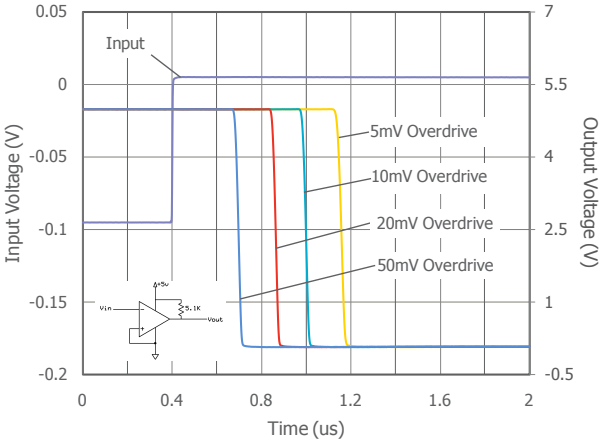
Response Time vs. Input Overdrive - Positive (CLC4550)



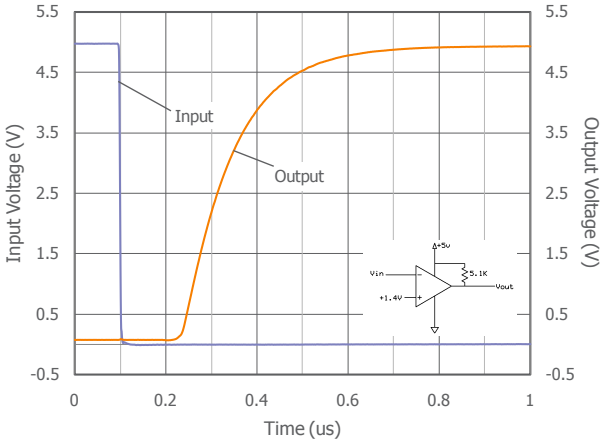
Response Time vs. Input Overdrive - Negative (CLC2550)



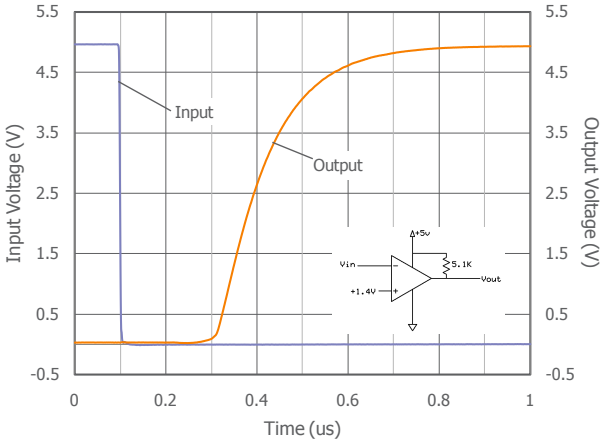
Response Time vs. Input Overdrive - Negative (CLC4550)



LS Response Time vs. Input Overdrive - Pos. (CLC2550)



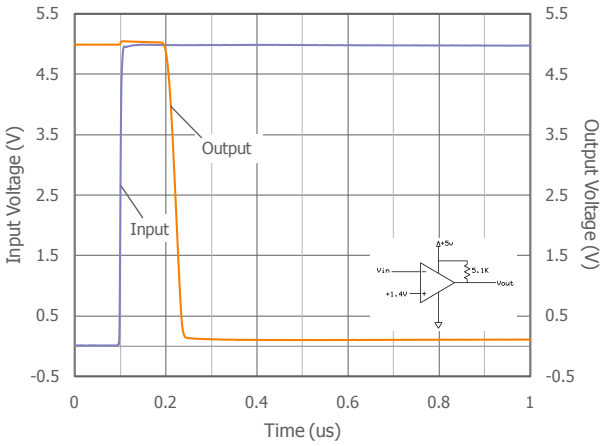
LS Response Time vs. Input Overdrive - Pos. (CLC4550)



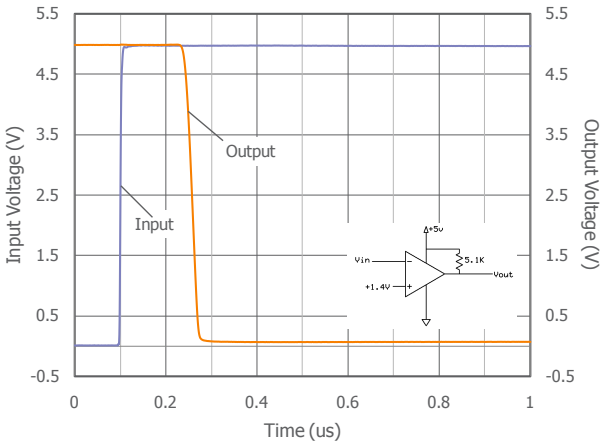
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = +5V, -V_S = GND unless otherwise noted.

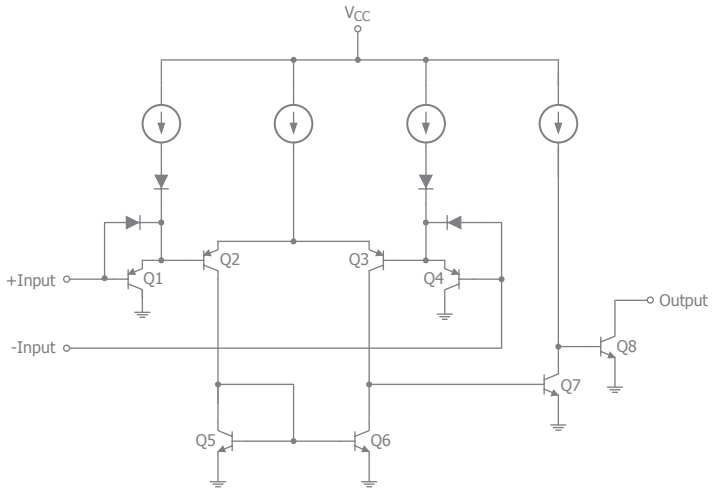
LS Response Time vs. Input Overdrive - Neg. (CLC2550)



LS Response Time vs. Input Overdrive - Neg. (CLC4550)



Functional Block Diagram



Application Information

The CLCx550 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be tied to the negative supply. The bias network of the CLCx550 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 2V DC to 30V DC. It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3V DC (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the CLCx550 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the CLCx550 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω RSAT of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	CLC2550
CEB018	CLC4550

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-14. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

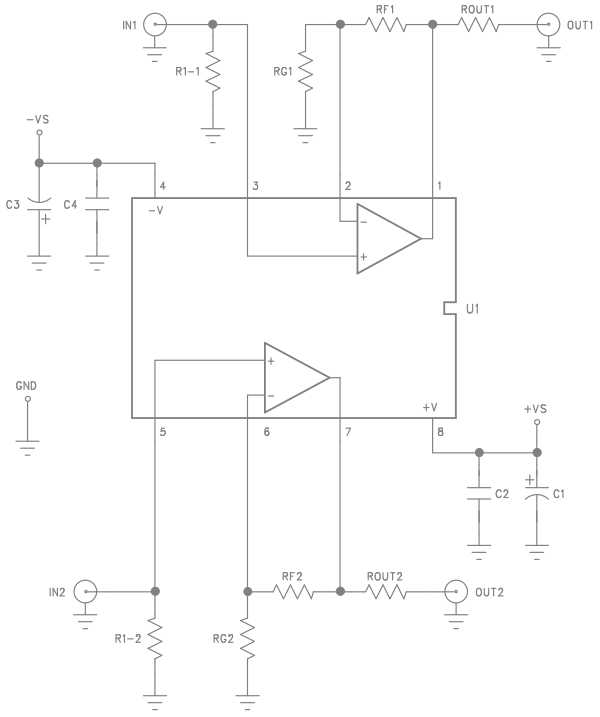


Figure 9. CEB006 Schematic

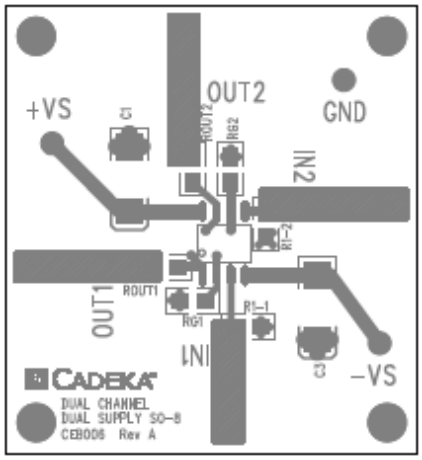


Figure 10. CEB006 Top View

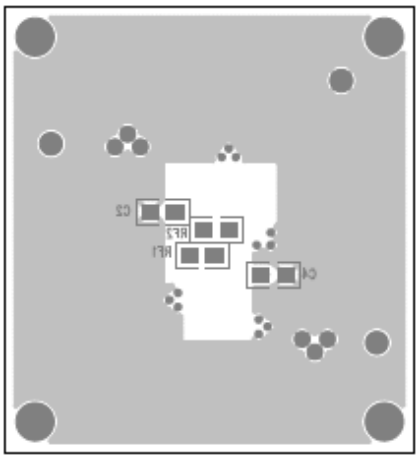


Figure 11. CEB006 Bottom View

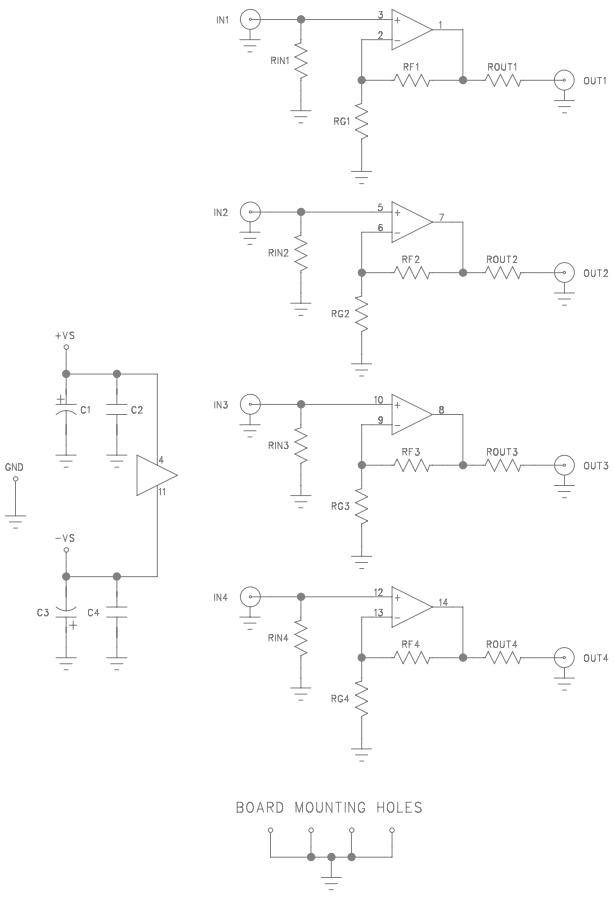


Figure 12. CEB018 Schematic

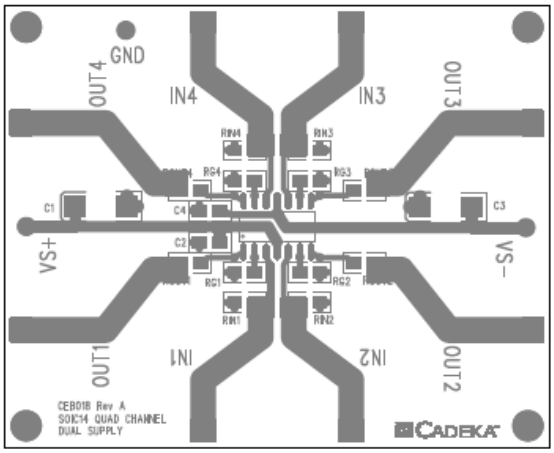


Figure 13. CEB018 Top View

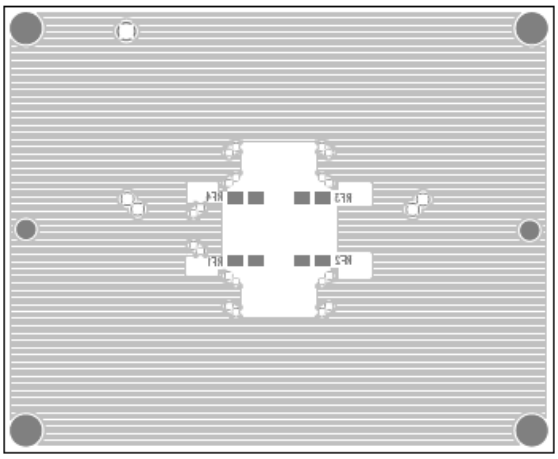


Figure 14. CEB018 Bottom View

Typical Applications

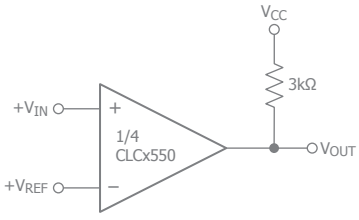


Figure 15. Basic Comparator

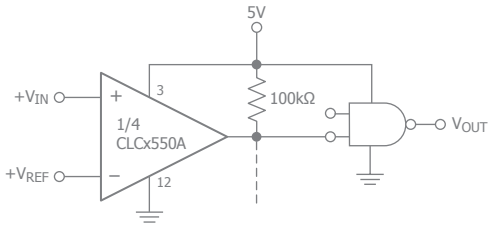


Figure 16. Driving CMOS

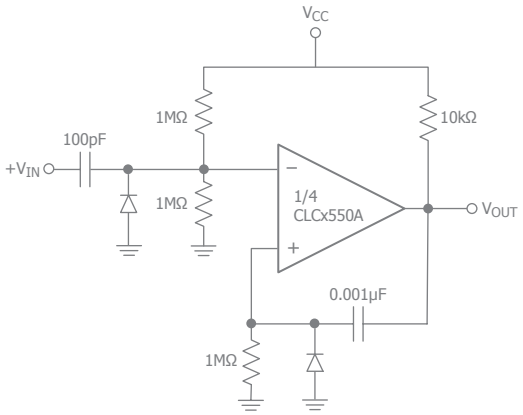


Figure 17. One Shot Multivibrator

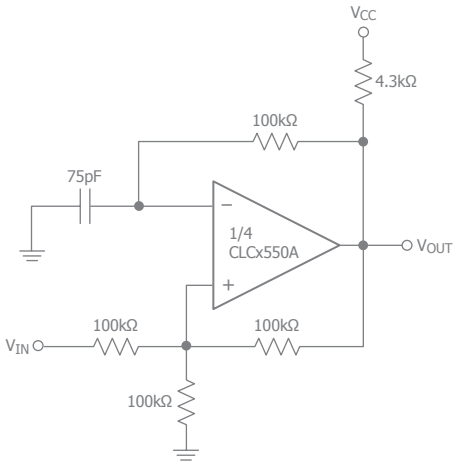
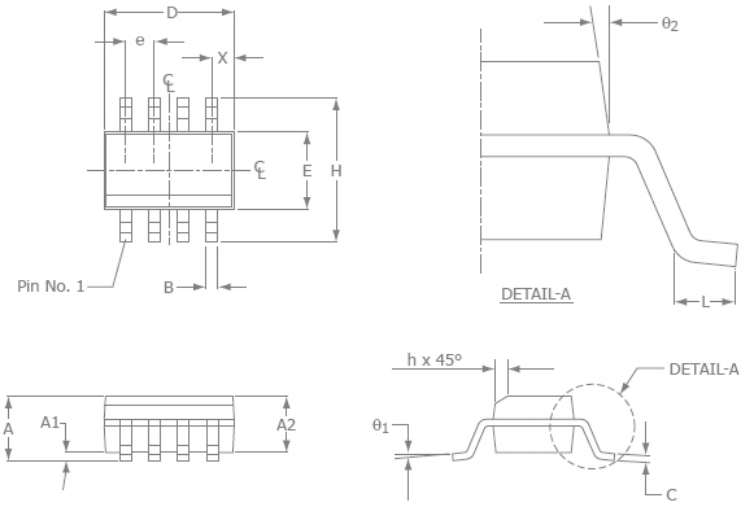


Figure 18. Squarewave Oscillator

Mechanical Dimensions

SOIC-8 Package

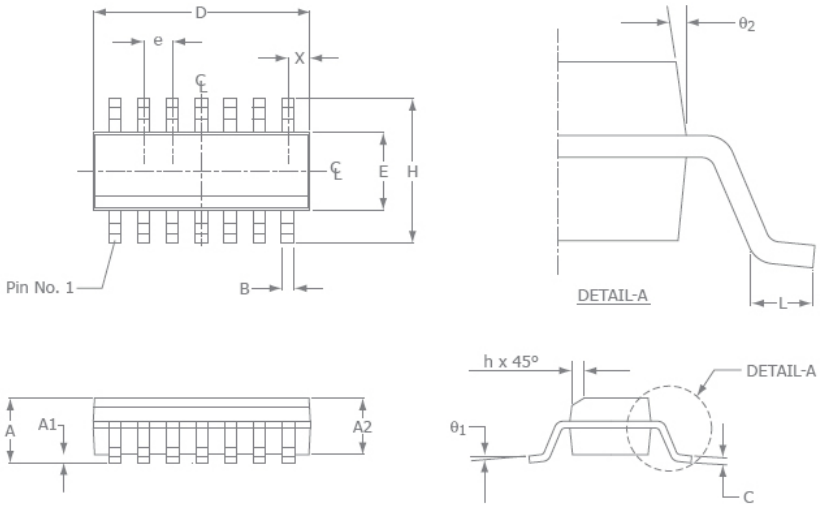


SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

SOIC-14 Package



SOIC-14		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	8.56	8.74
E	3.84	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.51 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

For Further Assistance:

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